FIG. 1A

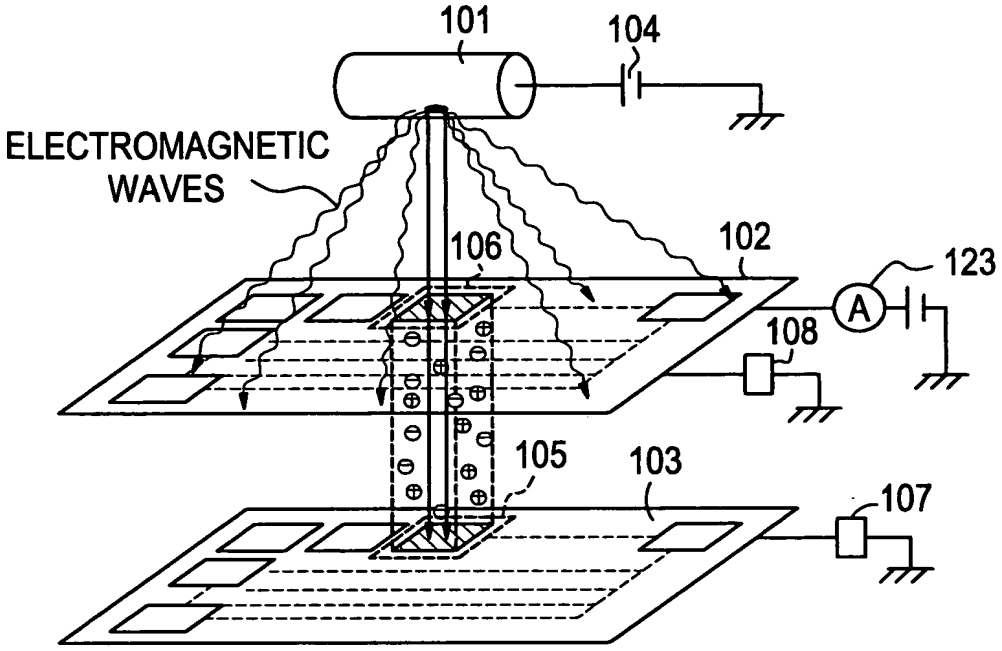

FIG. 1B

ENLARGED DIAGRAM OF 105

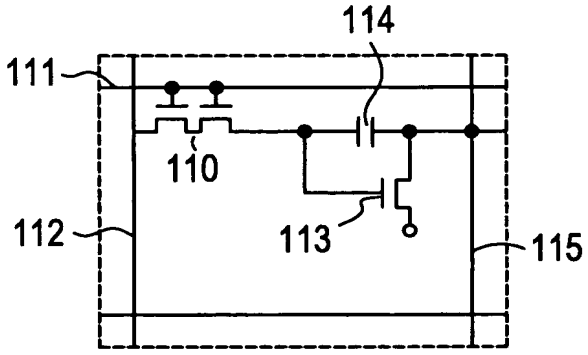

FIG. 1C

ENLARGED DIAGRAM OF 106

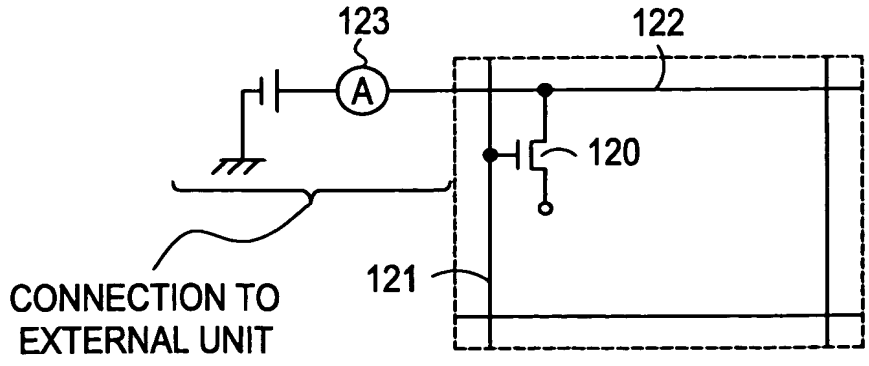

FIG. 2A

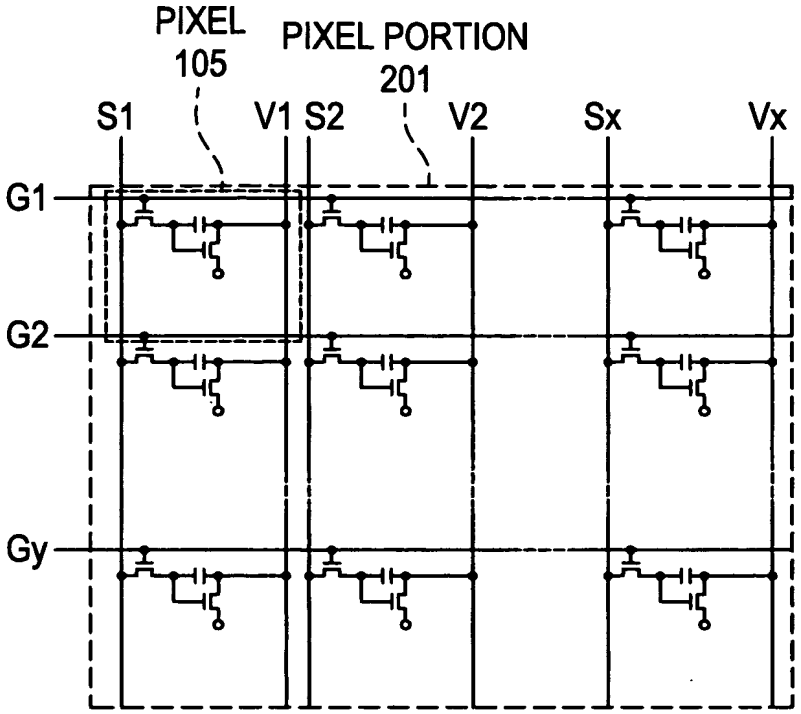
PIXEL
105
PIXEL PORTION
201
S1
V1
S2
V2
Sx
Vx
G1
G2
Gy

FIG. 2B

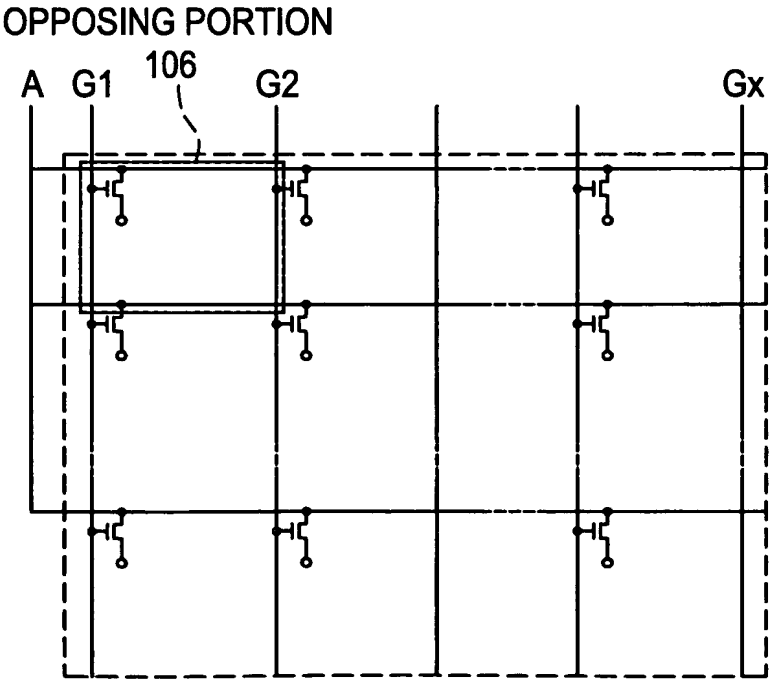
OPPOSING PORTION
106
A
G1
G2
Gx

FIG. 3A

(1, 1)	(2, 1)	(3, 1)	(4, 1)		(x-1, 1)	(x, 1)
(1, 2)	(2, 2)	(3, 2)	(4, 2)		(x-1, 2)	(x, 2)
(1, 3)	(2, 3)	(3, 3)	(4, 3)		(x-1, 3)	(x, 3)
(1, 4)	(2, 4)	(3, 4)	(4, 4)		(x-1, 4)	(x, 4)
(1, y-1)	(2, y-1)	(3, y-1)	(4, y-1)		(x-1, y-1)	(x, y-1)
(1, y)	(2, y)	(3, y)	(4, y)		(x-1, y)	(x, y)

FIG. 3B

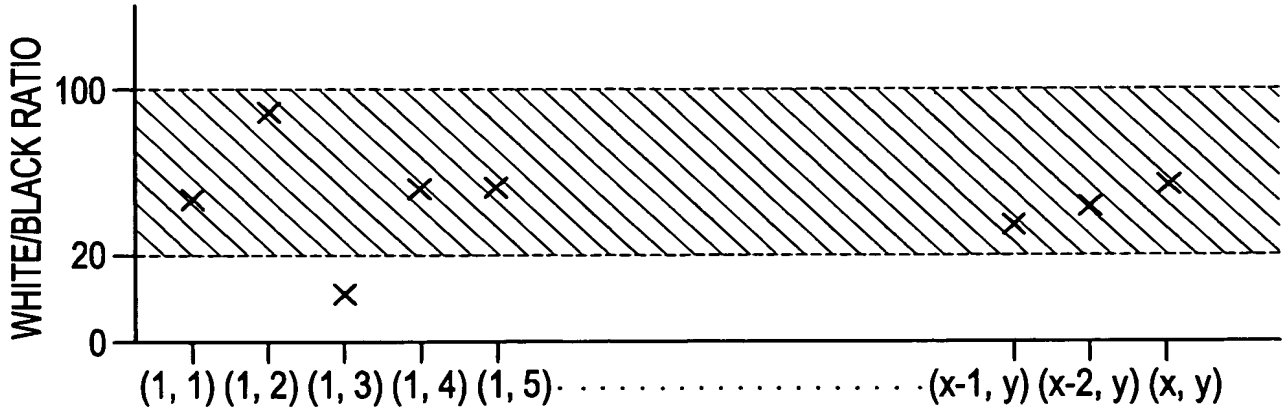

FIG. 4A

FORMATION OF ISLAND SEMICONDUCTOR LAYER, GATE-INSULATING FILM, AND FIRST AND SECOND CONDUCTING FILMS FOR GATE ELECTRODES

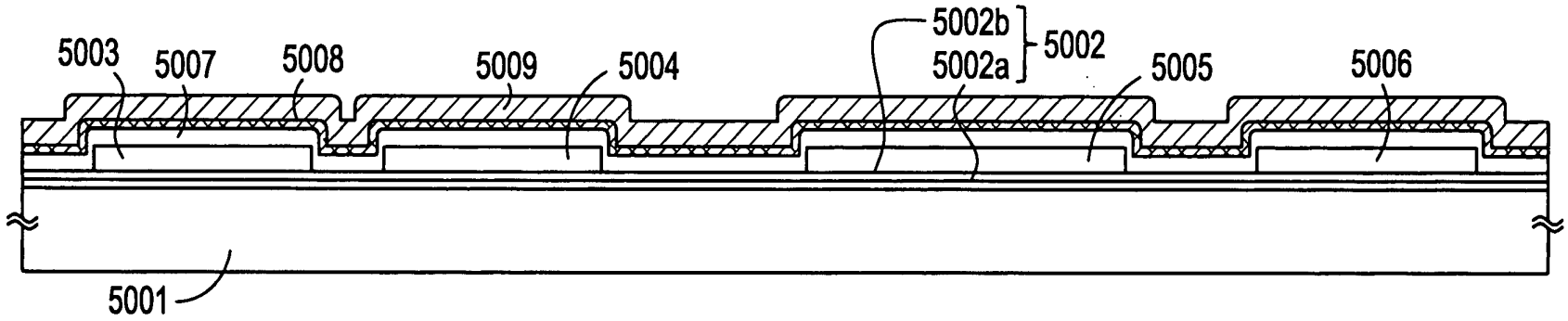

FIG. 4B

FIRST ETCHING AND FIRST DOPING

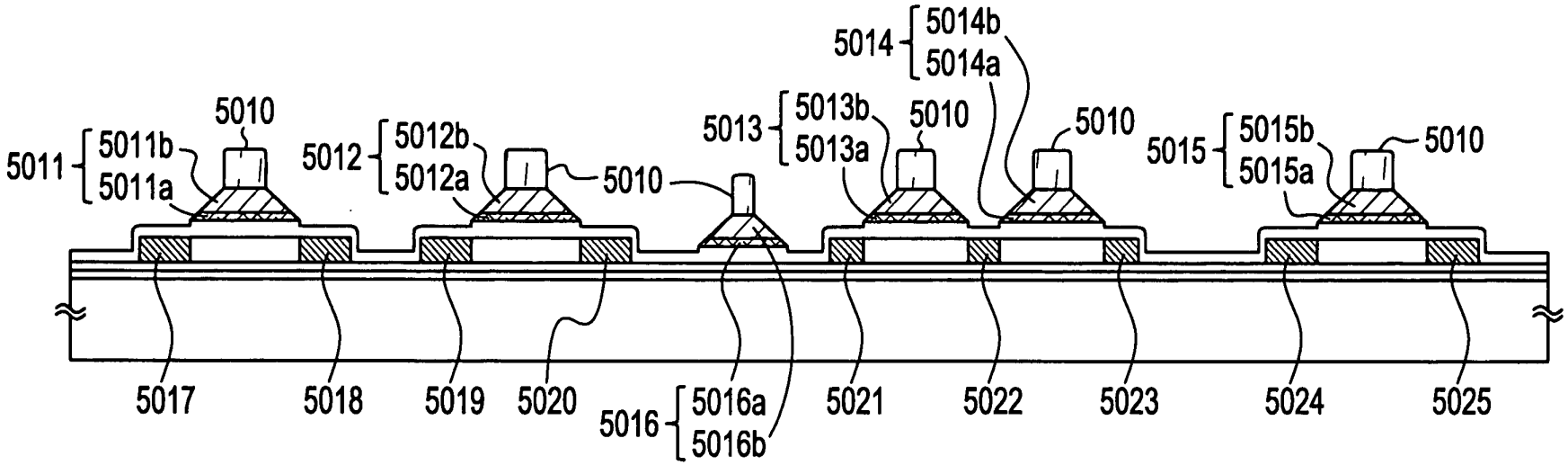

FIG. 4C
SECOND ETCHING

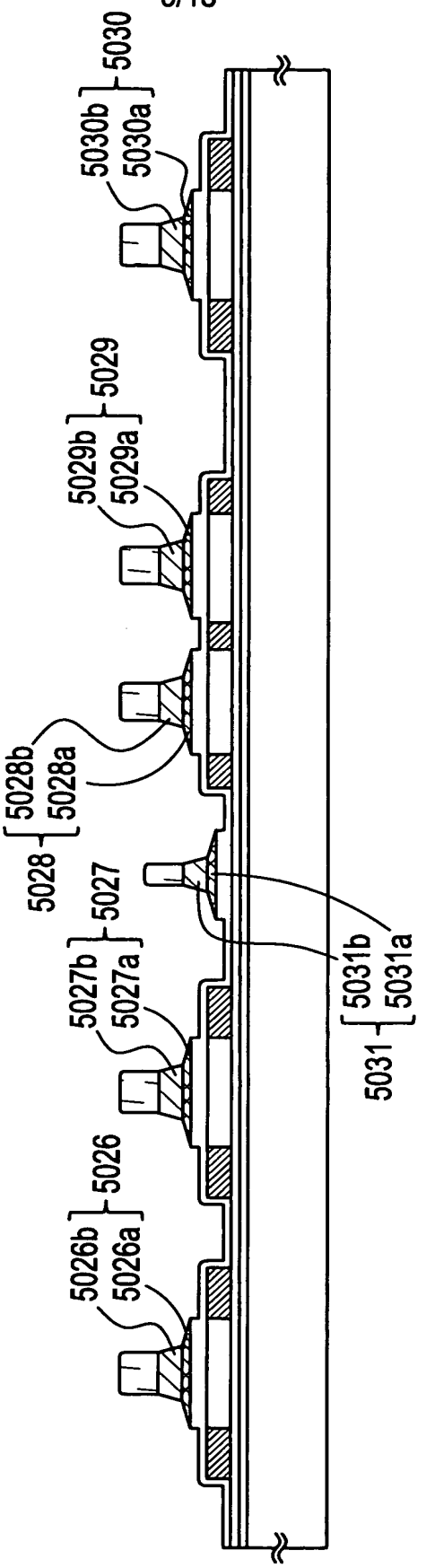

FIG. 5A
SECOND DOPING

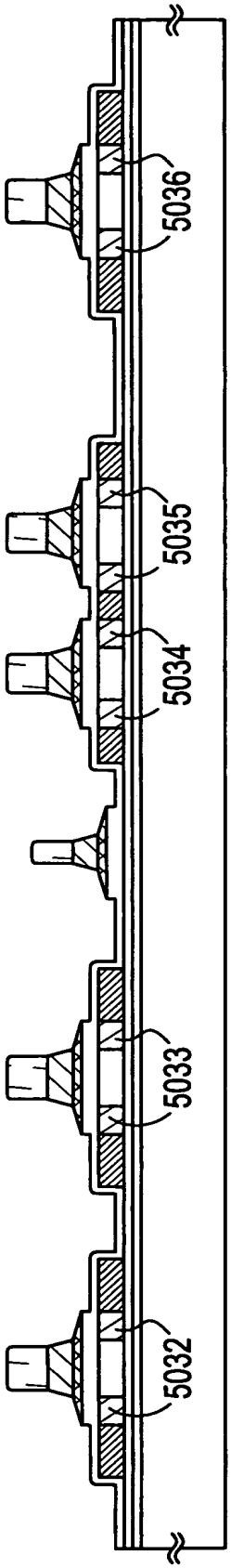

FIG. 5B
THIRD ETCHING

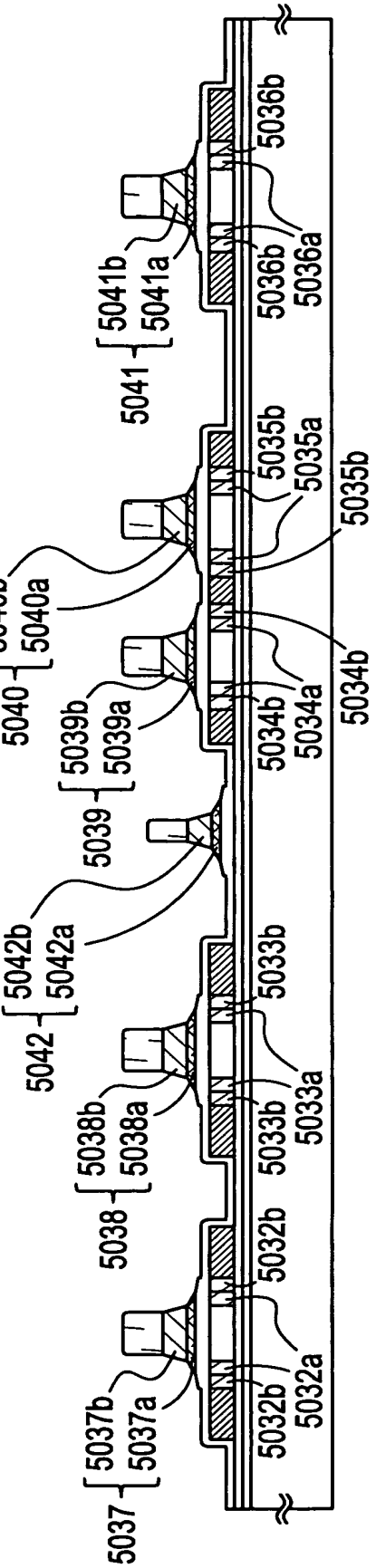

FIG. 5C
THIRD DOPING

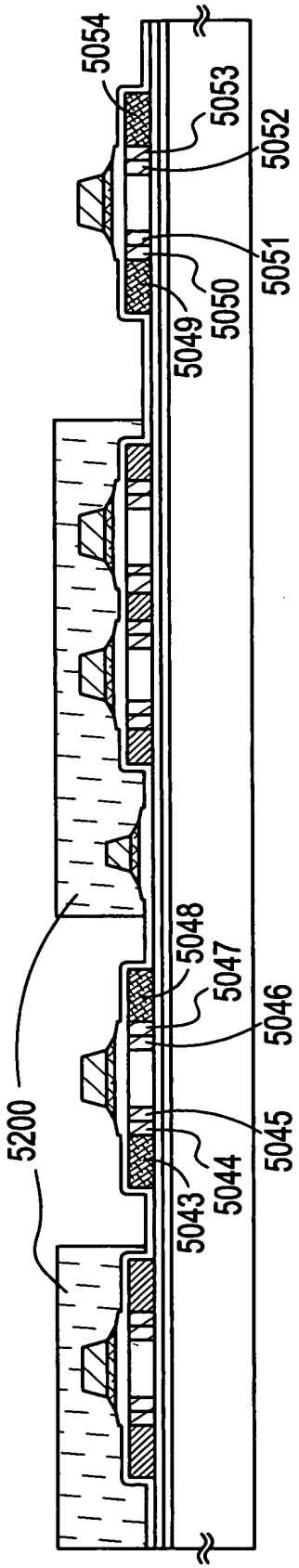

FIG. 6A

FORMATION OF THE FIRST AND SECOND INTERLAYER-INSULATING FILMS, WIRINGS AND PIXEL ELECTRODES

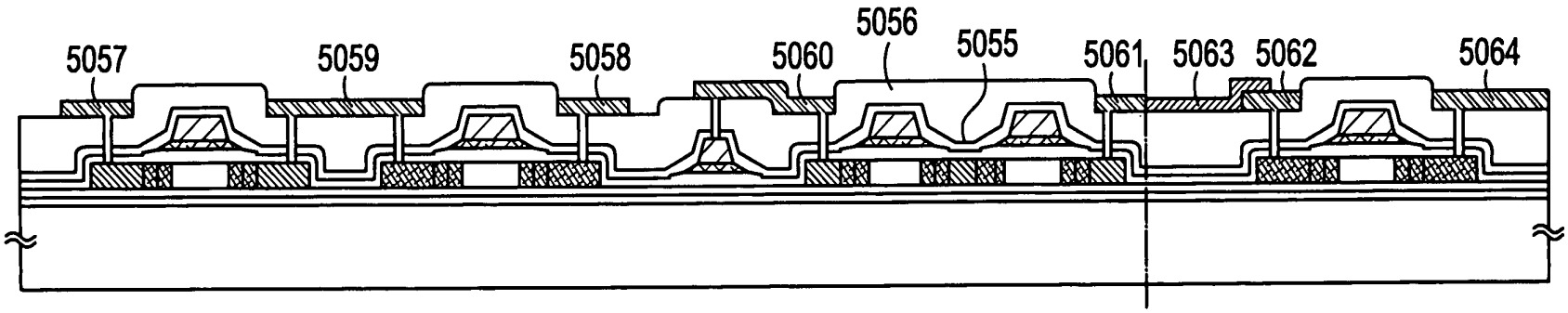

FIG. 6B

FORMATION OF THE THIRD INTERLAYER-INSULATING FILM, EL LAYER, CATHODES AND PASSIVATION FILM

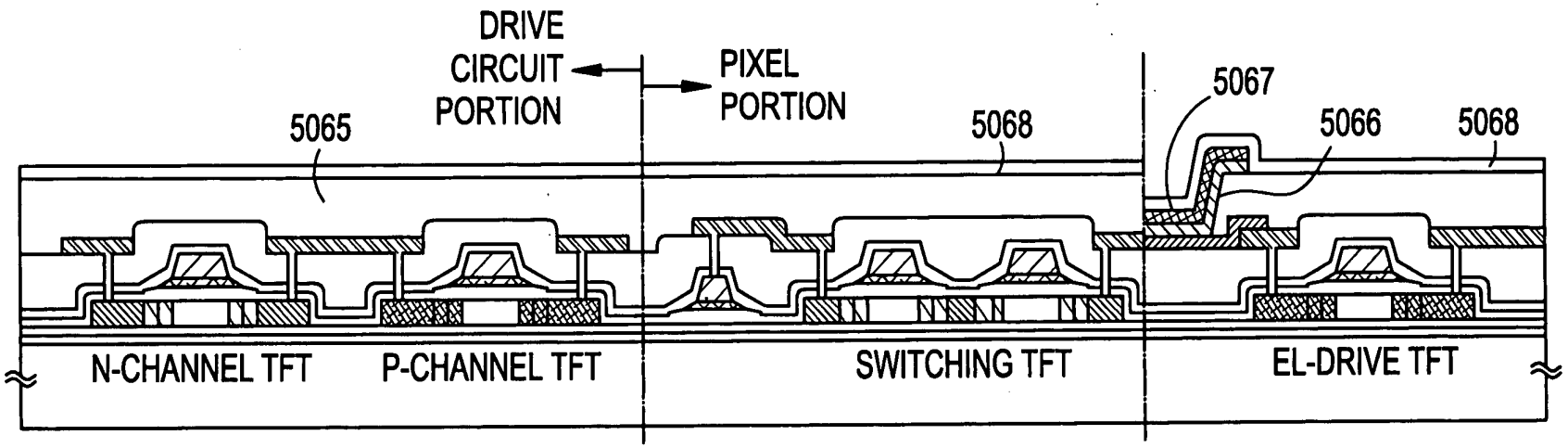

FIG. 7A

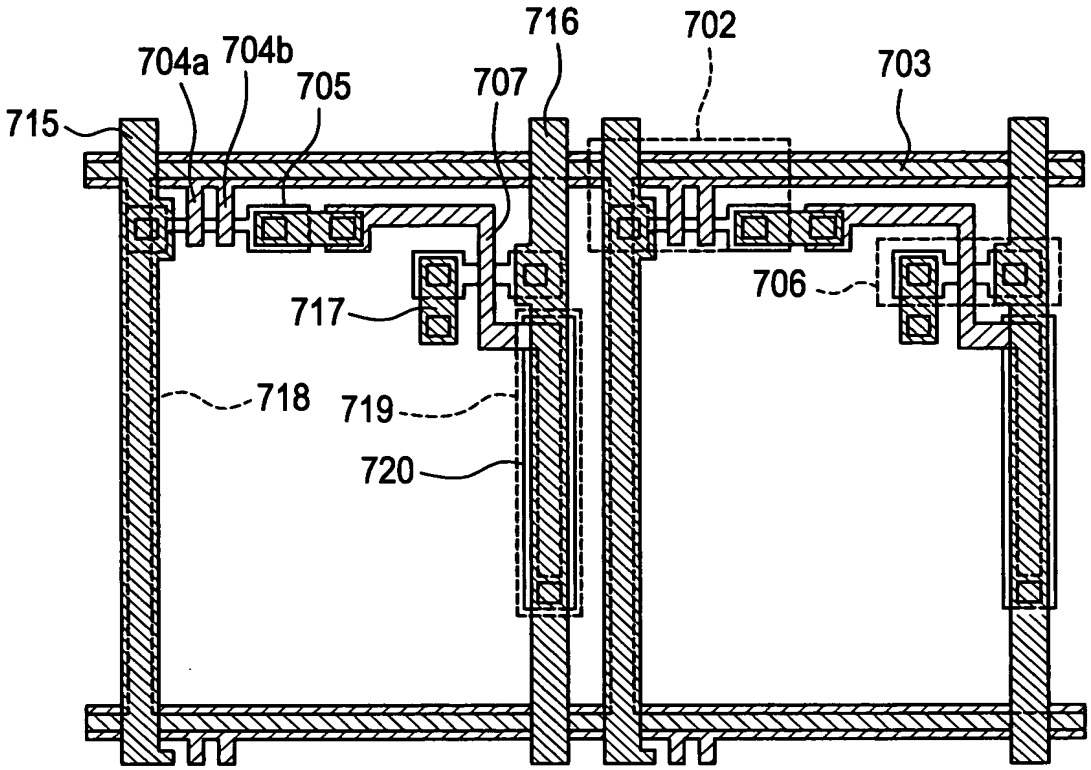
716
702
704a
704b
705
707
703
715
706
717
718
719
720

FIG. 7B

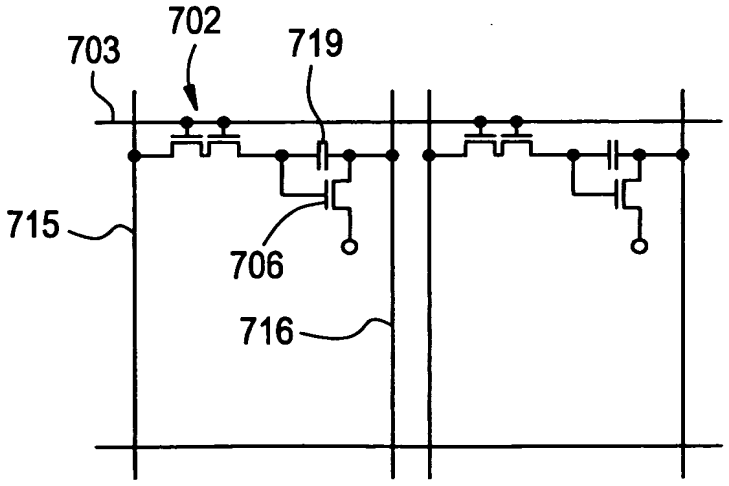
703
702
719
715
706
716

FIG. 8A

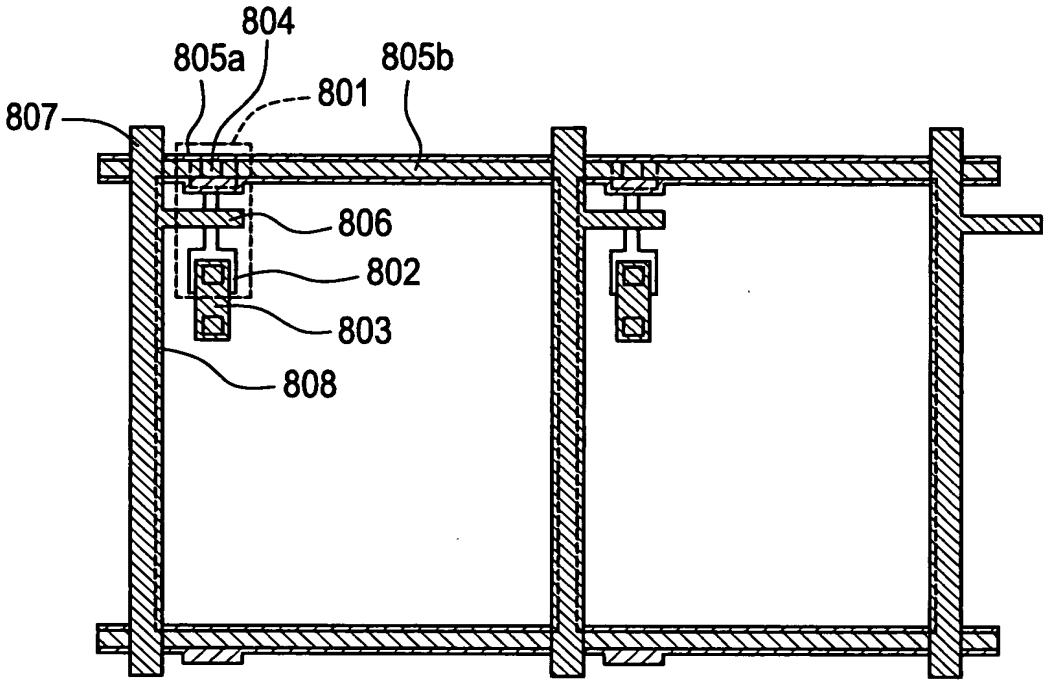

FIG. 8B

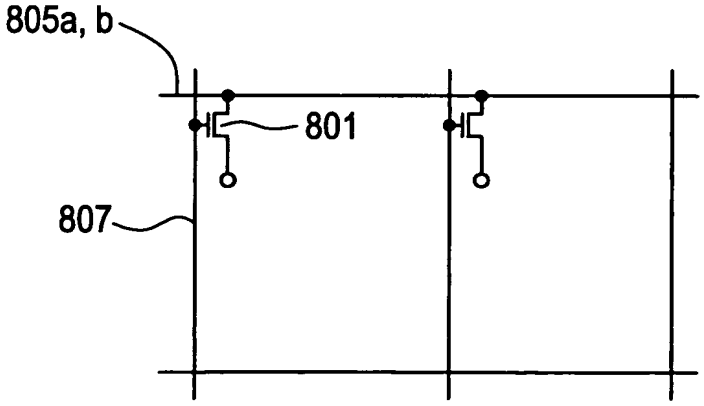

FIG. 9

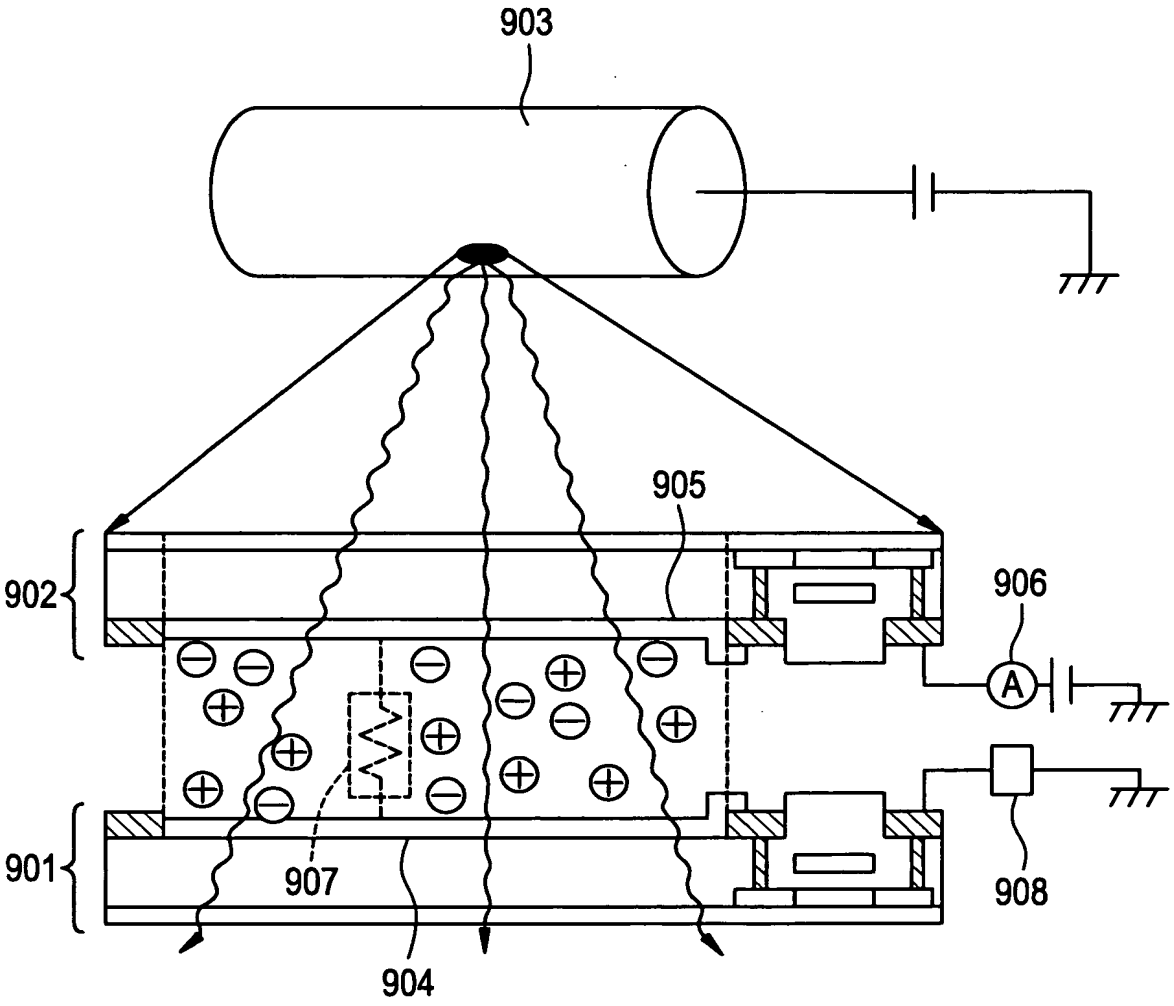

FIG. 10

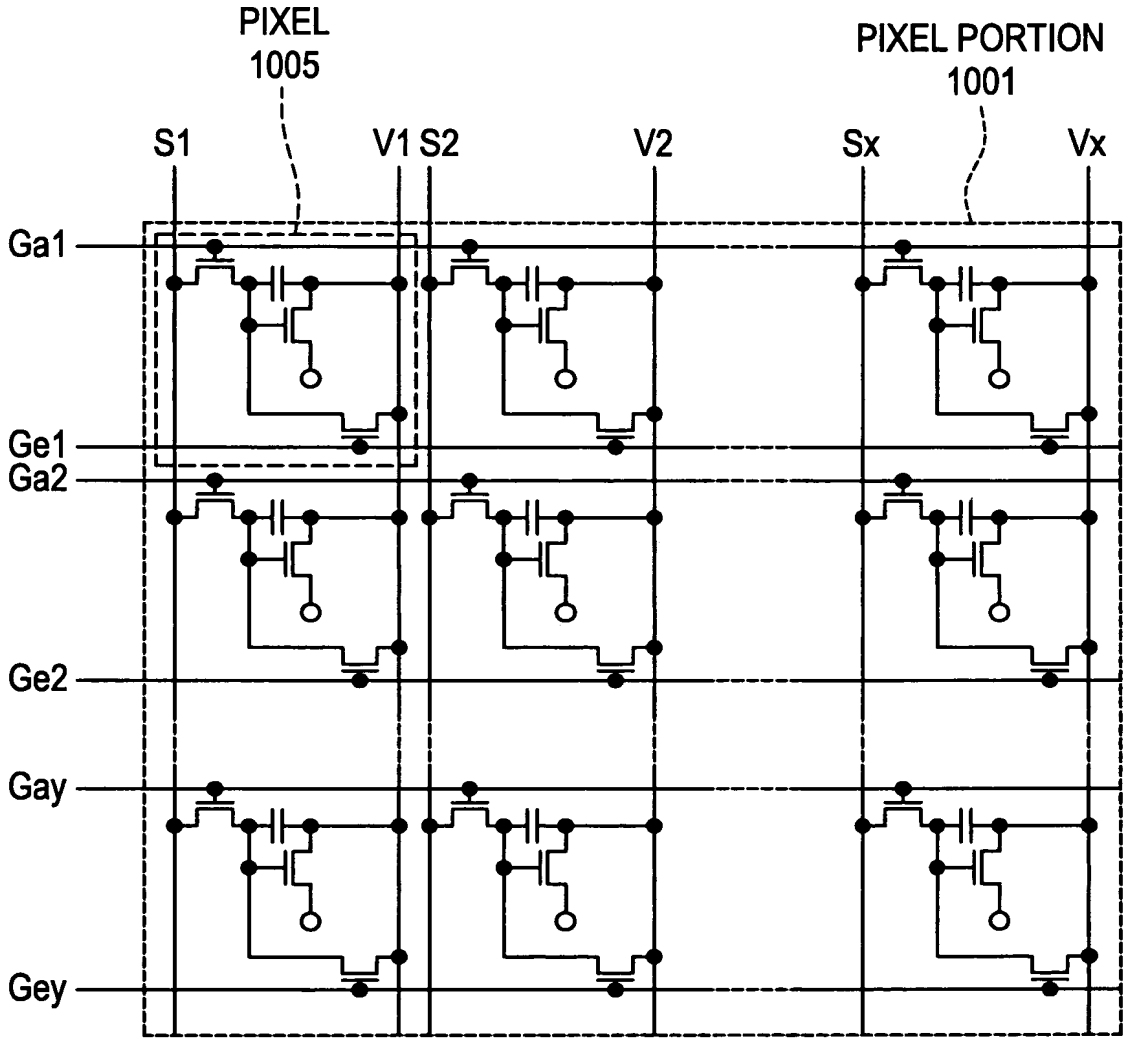
PIXEL
1005
PIXEL PORTION
1001
S1
V1
S2
V2
Sx
Vx
Ga1
Ge1
Ga2
Ge2
Gay
Gey

FIG. 11

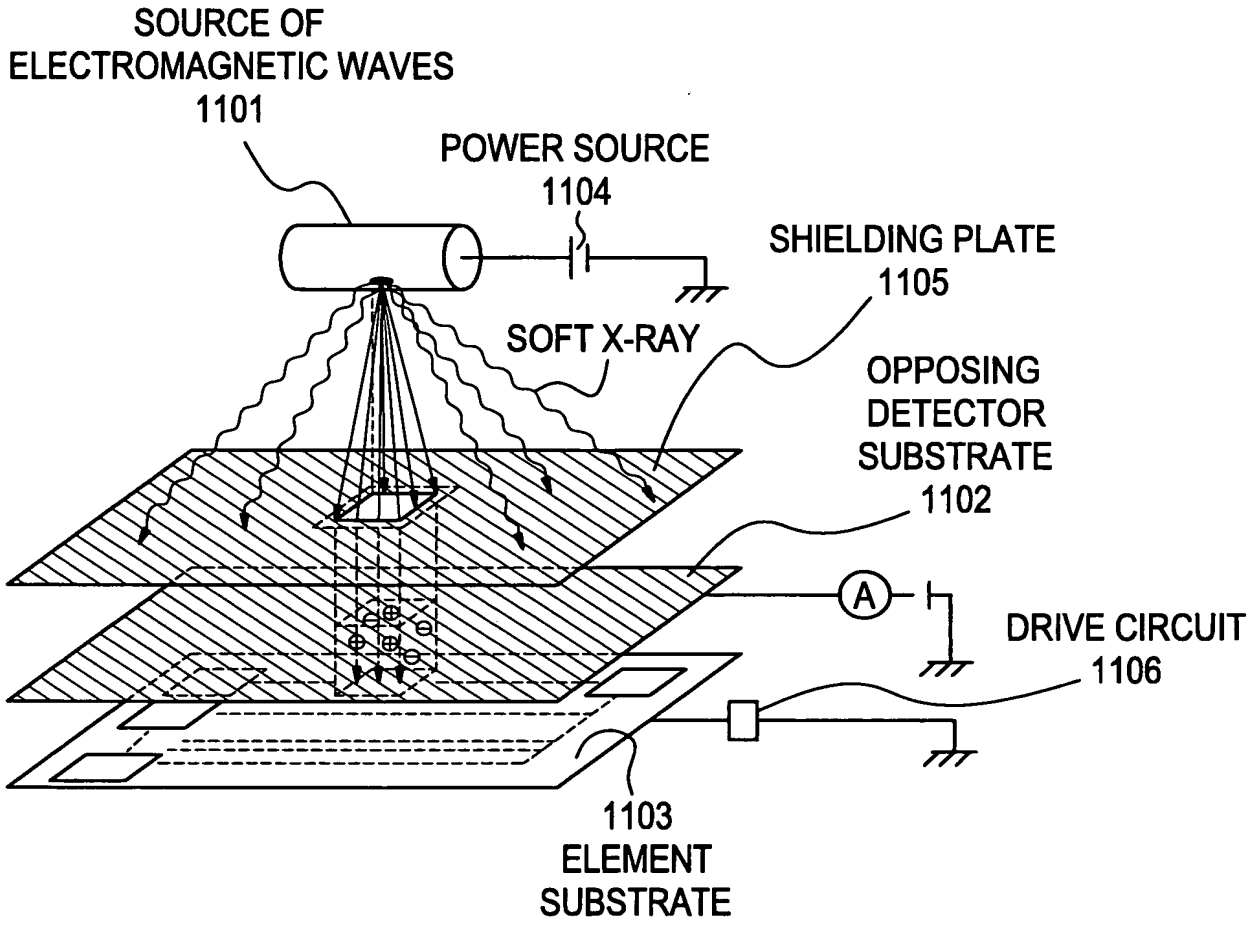
SOURCE OF
ELECTROMAGNETIC WAVES
1101
POWER SOURCE
1104
SHIELDING PLATE
1105
SOFT X-RAY
OPPOSING
DETECTOR
SUBSTRATE
1102
A
DRIVE CIRCUIT
1106
1103
ELEMENT
SUBSTRATE

FIG. 12

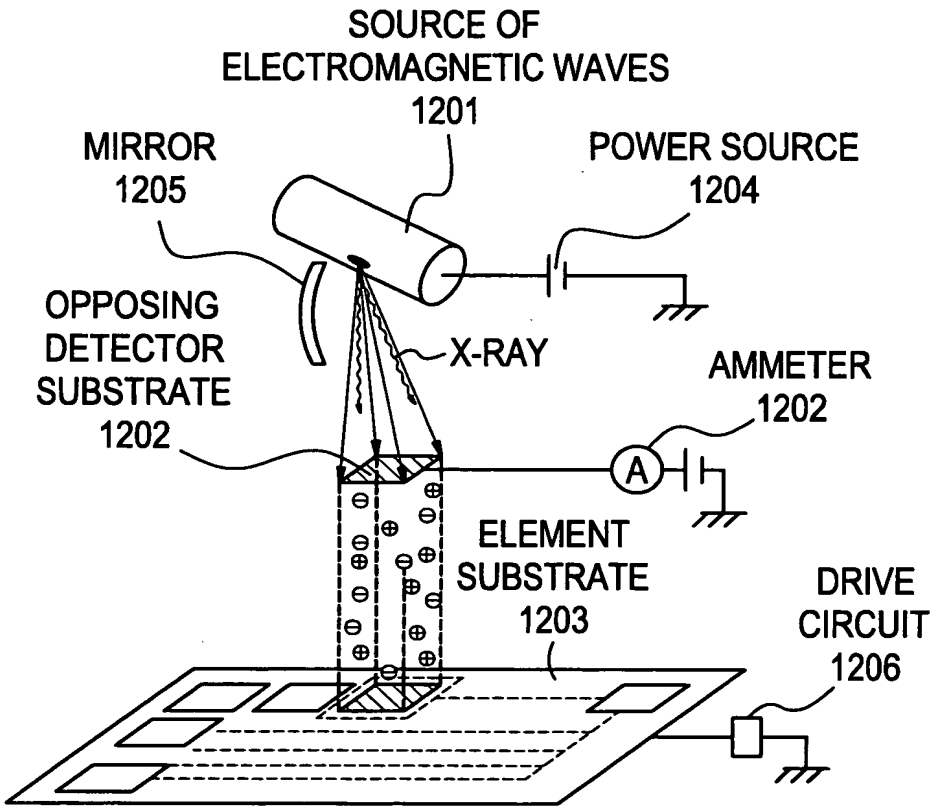
SOURCE OF
ELECTROMAGNETIC WAVES
1201
MIRROR
1205
POWER SOURCE
1204
OPPOSING
DETECTOR
SUBSTRATE
1202
X-RAY
AMMETER
1202
A
ELEMENT
SUBSTRATE
1203
DRIVE
CIRCUIT
1206

FIG. 13A

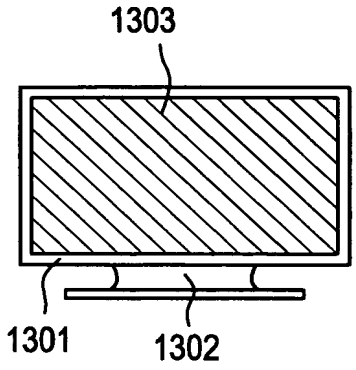

FIG. 13B

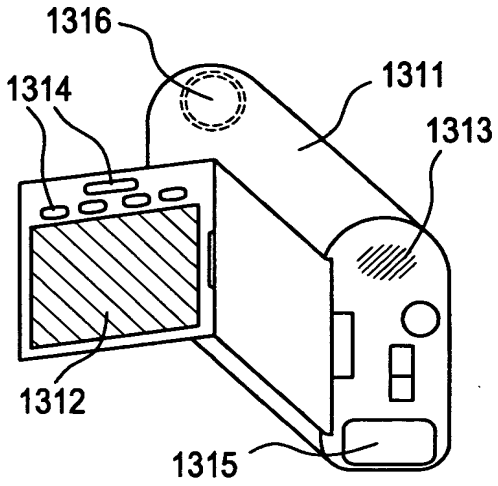

FIG. 13C

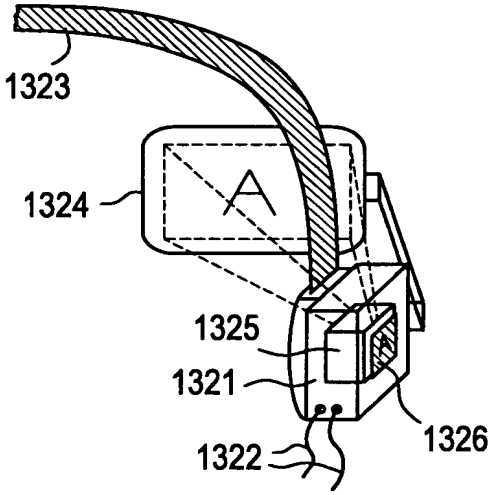

FIG. 13D

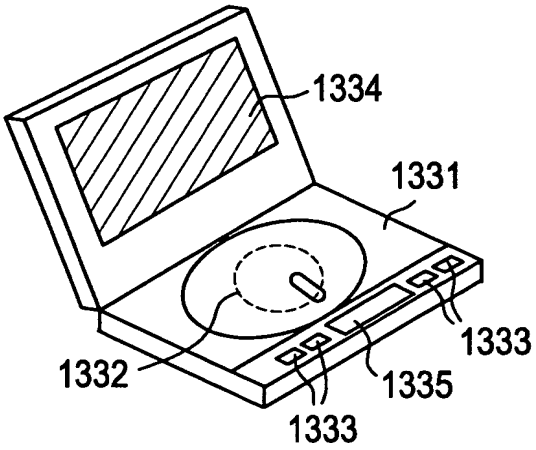

FIG. 13E

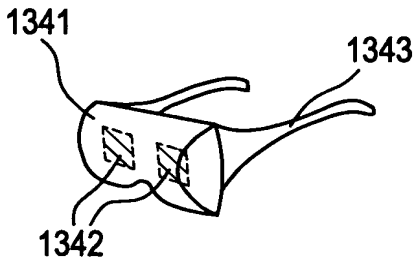

FIG. 13F

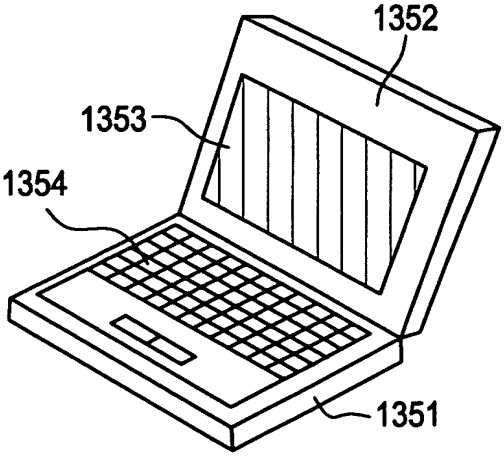

FIG. 14A

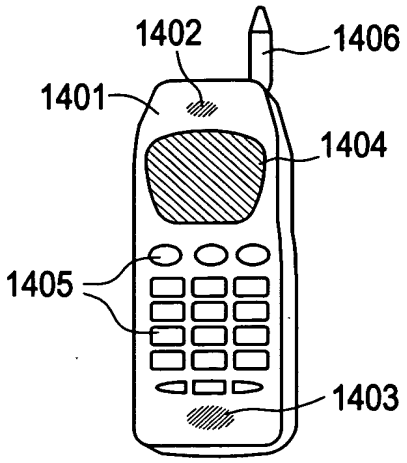

FIG. 14B

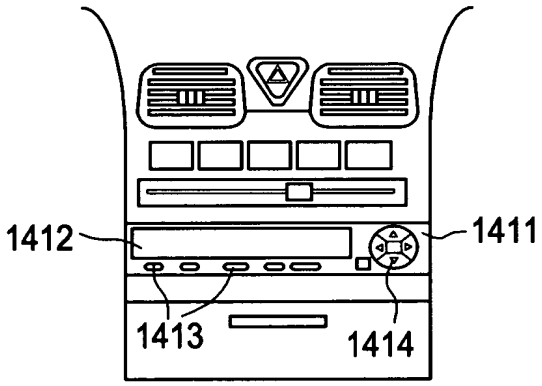

FIG. 14C

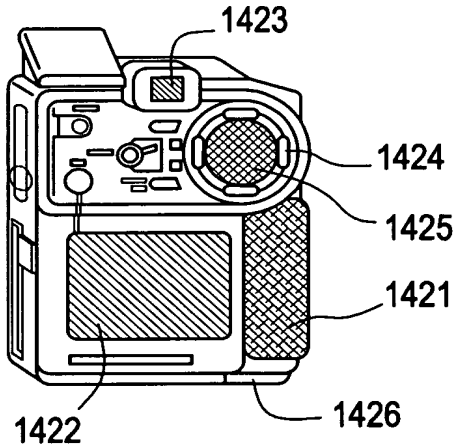

FIG. 15

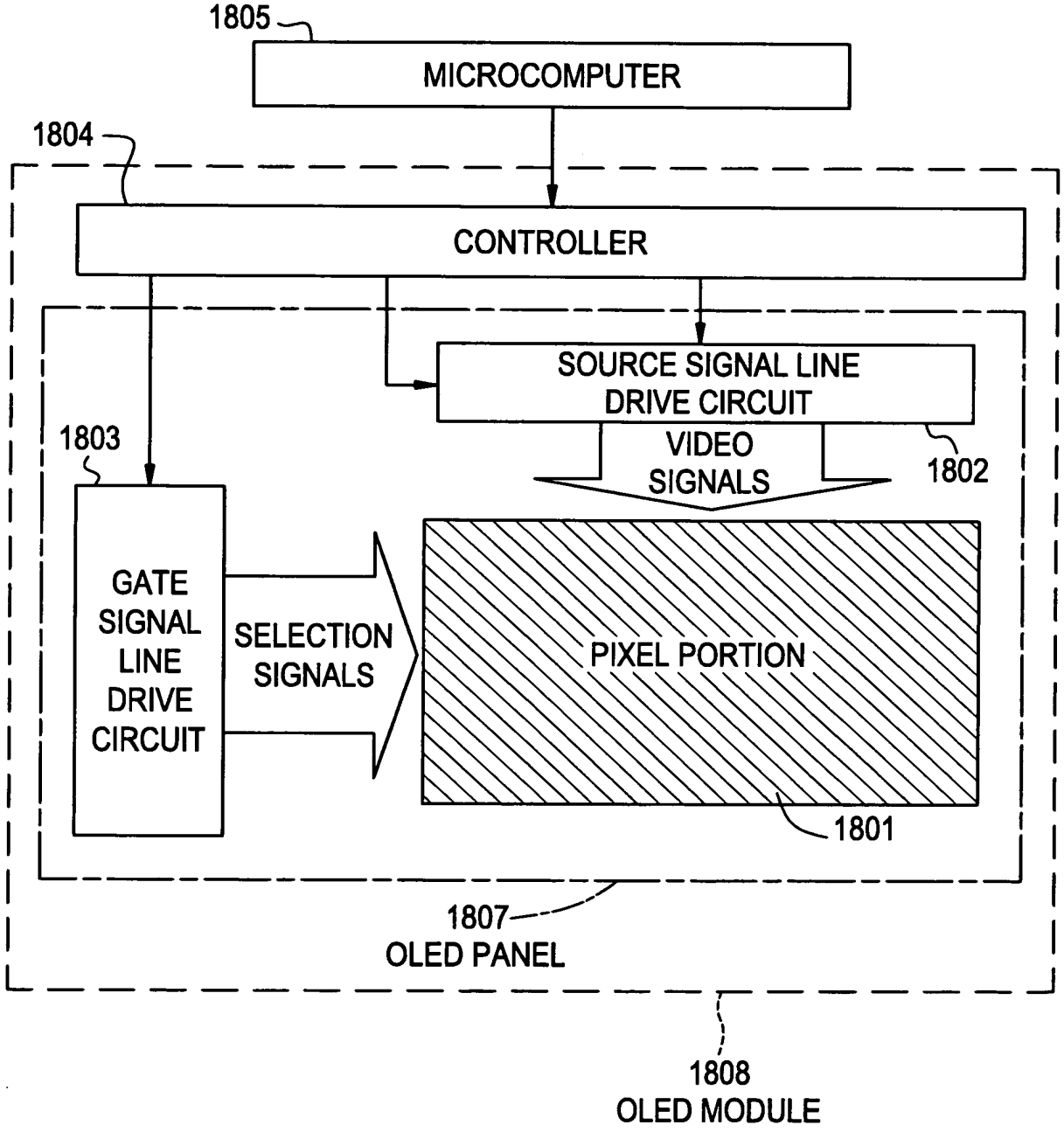
1805
MICROCOMPUTER
1804
CONTROLLER
SOURCE SIGNAL LINE
DRIVE CIRCUIT
VIDEO
SIGNALS
1802
1803
GATE
SIGNAL
LINE
DRIVE
CIRCUIT
SELECTION
SIGNALS
PIXEL PORTION
1801
1807
OLED PANEL
1808
OLED MODULE

FIG. 16A

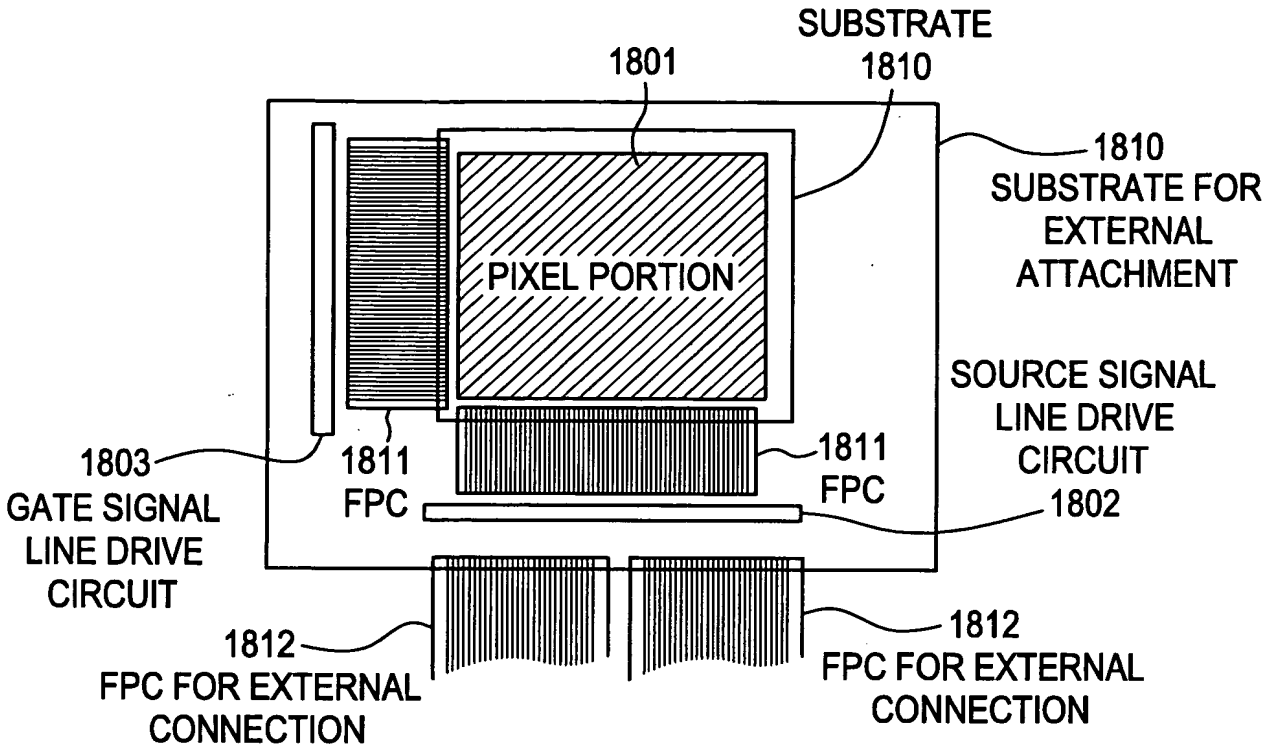

FIG. 16B